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U.S. Army Electronics Materiel Agency
Contract No. DA 36-039 SC-86733
Order No. 19055-PP-62-81-81

Pacific Semiconductors, Inc.

"A Subsidiary of Thompson Ramo Wooldridge Inc."
14520 So. Aviation Blvd. - Lawndale, California (Los Angeles County)

PSI

PACIFIC SEMICONDUCTORS, INC.

Research and Development Department
14520 South Aviation Blvd.
Lawndale, (Los Angeles County), California

FIRST QUARTERLY REPORT

PRODUCTION ENGINEERING MEASURE

Transistor, VHF, Silicon, Power (75W)

1 July 1962 to 30 September 1962

PSI Report No. 3000:47-Q-1

U.S. Army Electronics Materiel Agency
Contract No. DA 36-039 SC-86733
Order No. 19055-PP-62-81-81

This contract calls for the establishment of a limited production facility, the delivery of 2,475 25-watt, 100 megacycle transistors, and a study of the requirements for beginning a large scale production operation.

Prepared By

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Edited By

B. Rappaport

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SECTION I - ABSTRACT

Device design analysis, process improvements, and investigation of new contact techniques have been the major areas of activity during the first contract quarter. Additional work has been initiated in package analysis and package limitations. Test circuits have been designed for initial amplifier and oscillator testing and equipment for all Group A evaluation has been provided. The thermal path between crystal and stud has been under intensive investigation and significant improvement has been noted. The present processes have been reviewed, and diffusion photoresist and assembly area improvements and experiments have been initiated.

SECTION II - PURPOSE

The terms of the contract require the contractor to establish a limited production facility using prototype equipment capable of producing parts directed toward a rate of 200 transistors, that meet the applicable specifications, per 8-hour shift. During the contract period the contractor shall deliver a total of 2,475 transistors, of which 375 are engineering samples, 100 are pre-production samples, and 2000 are pilot production transistors. The 2000 transistors produced during the pilot run shall meet the applicable technical specifications. The specifications include performance as an amplifier - the transistor must be capable of 25 watts of power output at 100 megacycles with 10 db of power gain - and as an oscillator, the transistor must deliver 25 watts at a frequency of 100 megacycles. In addition, the package must be such that the transistor is electrically isolated from the case.

The prototype equipment required for the establishment of the pilot production run will be developed and supplied at the expense of the contractor.

Upon completion of the pilot production run, a Step II Study will be made to determine the requirements of a manufacturing facility capable of producing 50,000 units per month meeting

the applicable technical specifications and based on one 8-hour shift per day. The necessary plans and schedules required to establish the production capability based upon equipment capacity and pilot production yields shall be incorporated in the Step II Study.

SECTION III - TECHNICAL DISCUSSION AND DATA

Chapter 1

Introduction

It is the objective of the contract to conduct the engineering and processing work needed to establish a pilot production facility for producing 2,000 25-watt, 100-megacycle transistors that meet the Signal Corps Technical Requirement SCS-129 dated 12 February 1962, (See Appendix), or a modification of same that is mutually agreeable to the U.S. Army Electronics Material Agency and the contractor. The contract is a production engineering measure utilizing the 25W-100MC transistor developed under a Research and Development contract sponsored by the U.S. Army Signal Corps, Contract No. DA 36-039 SC-87342.

To accomplish these objectives an extensive program in product improvement has been planned which will incorporate the following items: Device design analysis and updating the present 25W-100MC Research and Development including various diffusion process improvements, evaluation of metallic contacts, evaluation of metallic contacts over the oxide, and optimization of the starting material with planned investigation of epitaxial material to replace the presently incorporated collector contact diffusion.

A redesign of the package will be one of the major aspects of device improvement. Power dissipation capabilities and frequency limitations will be analyzed in detail, and the package design will be formulated on experimental results obtained with the present package as discussed in Chapter 2.

A complete product engineering facility will be introduced which will establish pilot line capabilities for this device. This will include complete equipment evaluation. Initial plans for the equipment structure of the pilot line are being formulated, but must await determination of new process changes.

At present, test circuitry for amplifier and oscillator performance has been designed and is undergoing testing.

Other test equipment has been constructed as well, and lists of process equipment intended for the pilot line production of the 25W-100MC transistor are being outlined. This will be discussed in Chapter 3.

Section VII identifies the personnel that will be involved in establishing a production engineering methods development of this transistor.

The Signal Corps Technical Requirements are shown in the Appendix

to this report and a partial discussion of each of the individual specifications within these requirements is undertaken in Paragraph 2.2 - Device Design.

CHAPTER 2

Device and Process Engineering

2.1 Introduction

In any sophisticated device such as featured in the 75 watt-PEM contract, the set of specifications upon which the circuit designer rests his designs is comprised of factors from three areas:

a) The initial area of theoretical device design as discussed in paragraph 2.2 of this chapter. It is shown herein that the device specifications asked for in the 75 watt-PEM contract are not unreasonable in the sense of asking more than the silicon transistor can produce. However, some question arises on the correct number to insert on a specification for h_{fe}. The question comes from certain anomalies experienced during power amplification testing. Data taken indicates that conventional theories for h_{fe} versus power gain do not hold true.

b) The area of packaging which can be dismissed with a wave of the hand under low power and low frequency conditions become vitally important at 25 watts of power output (75 watts total dissipation) and 100 megacycles. It is an absolute requirement that the device and package be designed for each other if optimum performance is to be gained. Paragraph 2.4 of this chapter discusses our current problems in this area.

c) Given a perfect design and a perfect package, the device is still only as predictable and reliable as the processes used in its construction. Paragraph 2.3 surveys areas of processing which are currently under investigation in connection with this contract. This list is by no means complete. One would be remiss if one did not consider each and every process used in the light of potential improvements in:

a) speed

b) yield

c) reliability of device

d) device performance

2.2 Device Design

The transistor design for the device to be produced under this contract is founded on that employed in producing a 25W-100MC device, developed under U.S. Army Signal Corps Research and Development Contract No. DA 36-039 SC-87342.*,** The differences between the design specifications in the two transistors is not severe and is discussed briefly in this section. For ease of reference, the required performance specifications are listed in the Appendix to this report.

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* See Figure 2.2.0, 2.2.1 at the end of this chapter for details of the device as currently constituted.

** See Figure 2.2.2, 2.2.3 for a drawing of the existing case.

The change in V_{CBO} - I_{CBO} specification from (V_{CBO} less than or equal to 170V at I_C = 100 mAdc) to (I_{CBO} less than or equal to 5 mAdc at V_{CB} = 180Vdc) is not major from the device point of view. Theoretically the bulk resistivity of the silicon starting material assures us of far lower leakages. In practice the manufacturer is limited not by bulk resistivity, but by his process techniques for surface protection and passivation. Except for isolated units it has been extremely difficult for anyone to approach the theoretical bulk leakage currents due to higher (by orders of magnitude) surface leakages in silicon. During the coming months it is intended that a large portion of effort on the contract will be directed toward improving surface protection and passivation techniques allowing us to decrease bulk starting resistivity and leakages simultaneously. This same argument applies to the changes in I_{CES} from (less than or equal to 100 mAdc at 170V, less than or equal to 100 μA at 70 Vdc V_{CE}) to (less than or equal to 5 mAdc at 180V V_{CE}, less than or equal to 1 mAdc at V_{CE} = 70Vdc). The prime limitation is again not the physics, but the process.

One of the prime efforts for this contract in so far as device design analysis is concerned, will be in determining the relationship for this class of device between small-signal short-circuit forward-transfer ratio (h_{fe}) and power output and gain. To date the conventional formula for such relationships has not proven satisfactory. In particular, several units with h_{fe} less

than 0 db have given rated power (25W) at rated frequency bias and drive (100MC, 600mA, 80V, 2.5W input) during testing on the 25W-100MC Research and Development Contract. Until this evaluation is done there exists some doubt as to the exact value or values which should be placed on the specification for h_{fe} in the Appendix of this report.

The all important consideration of amplifier and oscillator performance at rated frequency bears considerable discussion and will be a featured subject of future quarterly reports.

Once final test results become available from the 200 units produced under U.S. Army Signal Corps Contract DA 36-039 SC-87342 (Research and Development) and the first 75 engineering samples under this contract, it will be possible to combine present theoretical computations with statistically valid test samples and provide a sound basis on which to project device design and package changes enhancing the device performance. For the present, one can say that the 25W-100MC or 75W PEM transistor is capable of exceeding the specifications in the Appendix of this report, and with improvements in the package and device design a substantial pilot line yield to these specifications is possible.

There exist a number of potential areas capable of improvement from the device designer's point of view. It would be convenient to be able to remove considerable heat from the top of the device

as well as through the collector contact region. If this were done it would be possible to improve frequency characteristics by changing the physical geometry of the device, and still keep the temperature of the PN collector base junction within reason. This, however, is primarily a packaging problem and so is discussed in Paragraph 2.4 of this chapter.

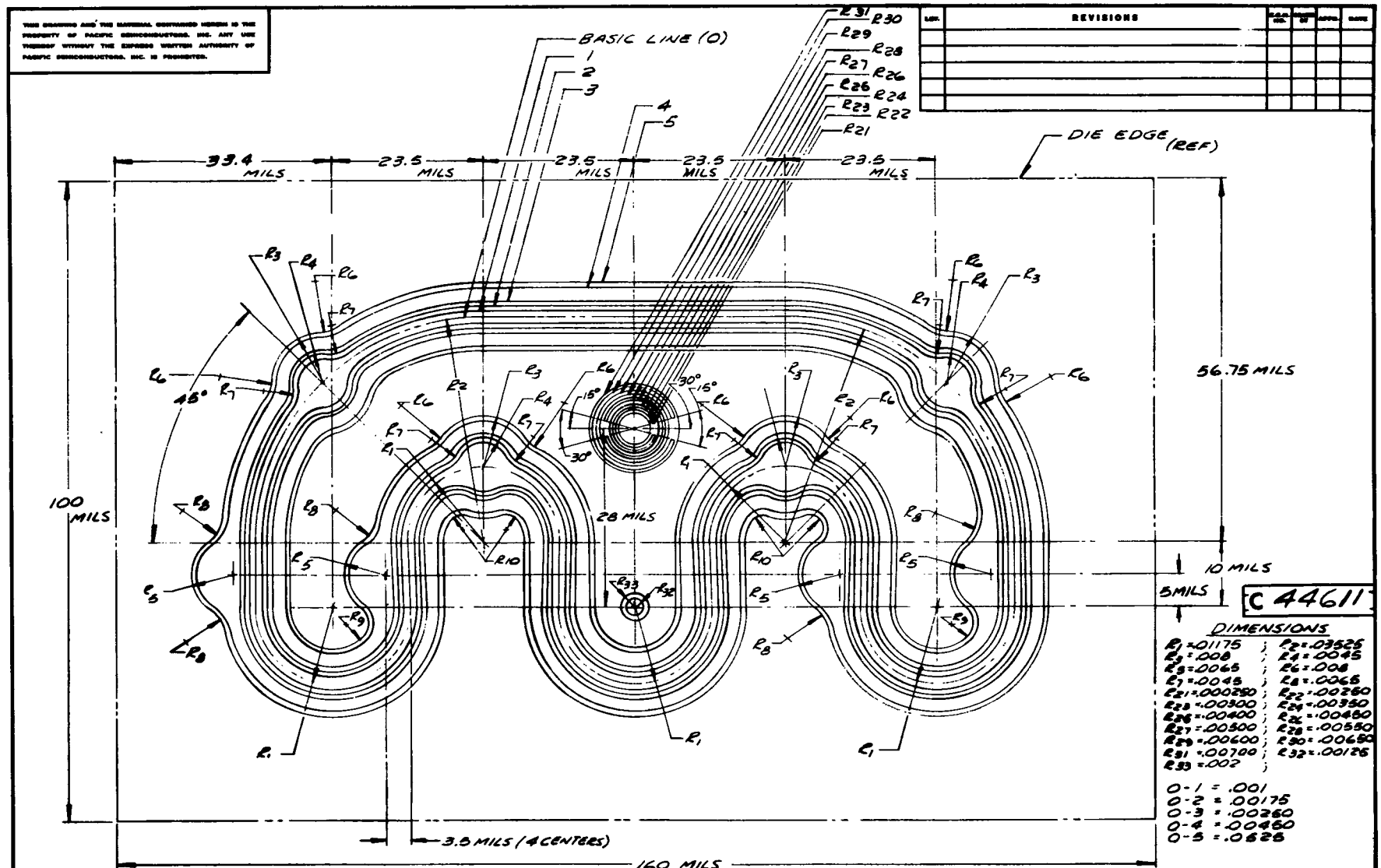
The introduction of epitaxial material also constitutes a device design change in that it gives a slightly simpler picture when an attempt is made to understand the dopant concentration curves in the emitter base region. A trade-off is necessary between frequency performance and emitter base breakdown. With the aid of an epitaxial region this trade-off becomes less critical. It would also be of assistance in eliminating the difficult problem of high $V_{CE(SAT)}$. With further improvement in surface processing and formation of oxides, it should also be possible to reduce the bulk resistivity now employed as a starting material and thereby produce a number of benefits, such as better frequency performance. The use of a narrower stripe width geometry for the transistor would have a beneficial effect on transistor performance, lowering the emitter and collector capacitance and increasing the f maximum.

In summation it is to be emphasized that at present the design of a silicon crystal for the 25W-100MC transistor used in the 75W-PEM is far better than the current packaging design. As a result, the principal initial improvements to be expected lie in the packaging area. Once the package, including both thermal

Emitter Length	402.1×10^{-3} inch
Emitter Width	3.5×10^{-3} inch
Emitter-Emitter Spacing Minimum	22×10^{-3} inch
Metallizing Width	2.0×10^{-3} inch
Collector Area	4504×10^{-6} inch^2
Dice Area	12850×10^{-6} inch^2
Resistivity	12 - 14 ohm/cm

FIGURE 2.2.0

Physical Parameters for 25W-100MC Transistor



C 44611

DIMENSIONS

R_1 = .01175	R_2 = .03525
R_3 = .008	R_4 = .0045
R_5 = .0065	R_6 = .008
R_7 = .0045	R_8 = .0065
R_{22} = .000250	R_{22} = .00260
R_{23} = .00300	R_{24} = .00350
R_{25} = .00400	R_{26} = .00450
R_{27} = .00500	R_{28} = .00550
R_{29} = .00600	R_{30} = .00650
R_{31} = .00700	R_{32} = .00125
R_{33} = .002	

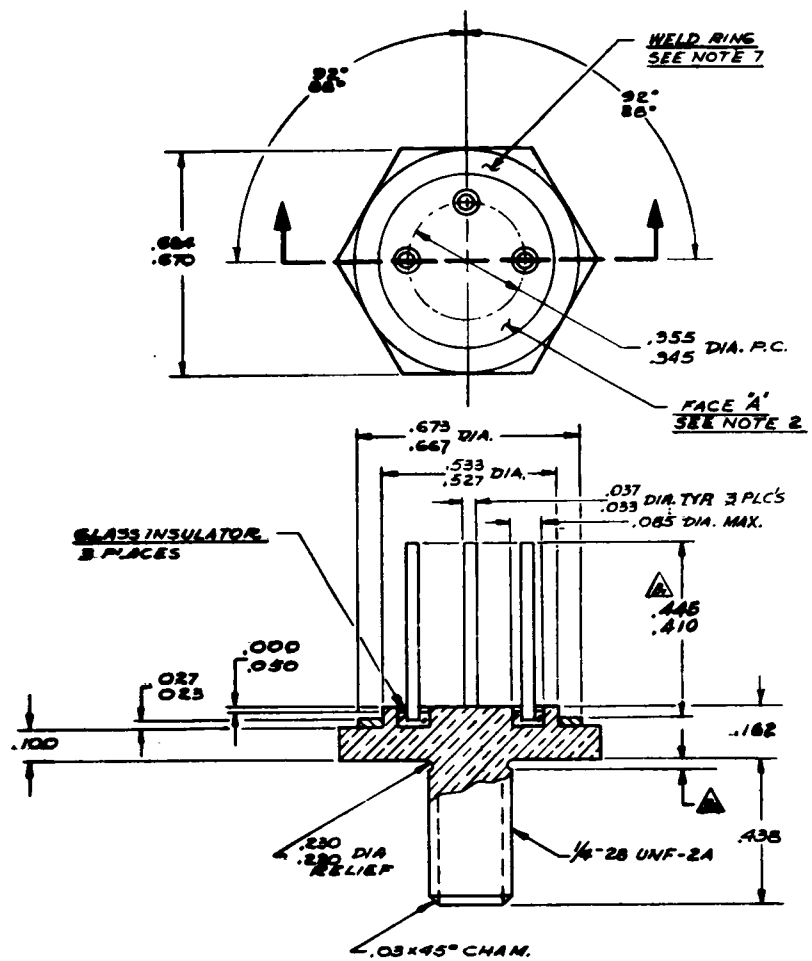
0-1 = .001
0-2 = .00175
0-3 = .00260
0-4 = .00460
0-5 = .0625

3. NOT SPECIFIED RADII ARE DETERMINED BY INCREASING OR DECREASING THE SPECIFIED RADII ACCORDING TO THE DIMENSIONS OF THE MAIN STRUCTURE DWG. NO. C 44611
2. THE CENTERS OF THE CONNECTING ARCS R_6, R_7, R_8 ARE DETERMINED FROM THE DIMENSIONS OF THE MAIN STRUCTURE DWG. NO. C 44611; ARCS R_9 & R_{10} TO BE TANGENTIAL TO RESPECTIVE CONNECTING ARCS
1. ALL WIDTH MEASUREMENTS TO BE SYMETRICALLY DETERMINED FROM BASIC LINE AS PER DIMENSIONS GIVEN

NOTES:

FIG. 2.2.1 OUTLINE OF 25 W, 100 MC AMPLIFIER

REVISIONS				
A	.365/.346 WAS .382/.360			
	B_1 WAS .238; B_2 DELETED G.H. 2-14			
	B_3 DELETED; RELIEF DIM. .238			

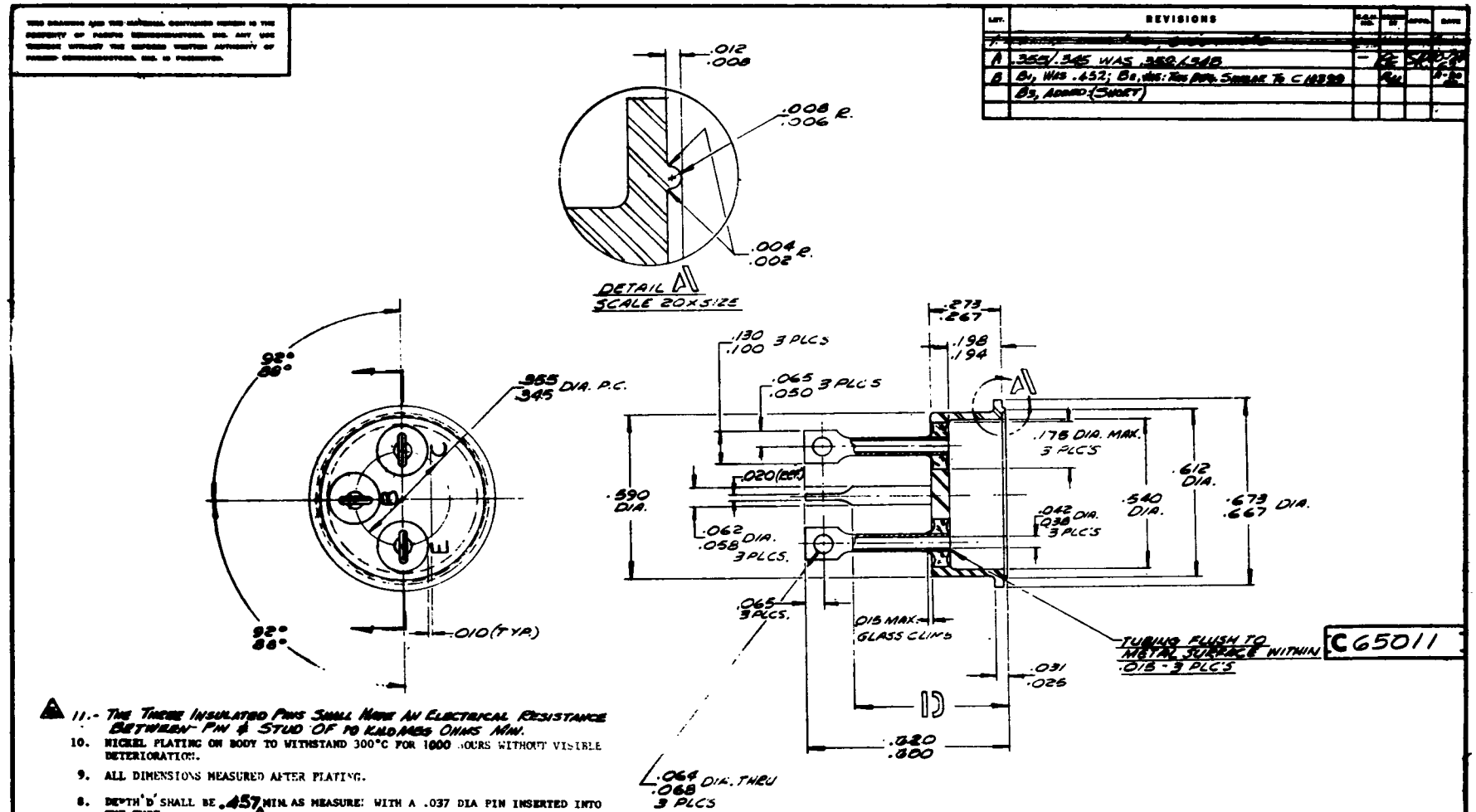


NOTES

1. BREAK ALL EDGES AND CORNERS .010 R. MAX.
2. FACE "A" TO BE FLAT WITHIN ± .001.
3. THE THREE INSULATED PINS SHALL HAVE AN ELECTRICAL RESISTANCE BETWEEN PIN AND STUD OF 10 KILOMEGOHMS MIN.
4. BEARING SURFACE UNDER HEAD TO BE FLAT WITHIN .001 MAX. AND SQUARE WITH THREAD C.L. WITHIN .003 T.I.R.
5. UNIT MUST WITHSTAND BRAZING. IN A REDUCING ATMOSPHERE WITH EASY-FLO 45 WITHOUT REMELTING OF BRAZING MATERIAL, CREATION OF VOIDS IN GLASS, OR DETERIORATION OF PLATING. PINS SHALL BE SUPPORTED DURING BRAZING OPERATION.
6. NO VOIDS ARE PERMISSIBLE (UNDER 10 POWER MAGNIFICATION) ON BRAZED OR GLASS SURFACE.
7. WELD RING TO BE LOW CARBON STEEL. SURFACE INDICATED TO BE FLAT WITHIN .001 T.I.R., AND PARALLEL TO THE UNDERSIDE OF THE HEX, ON THE CIRCUMFERENCE WITHIN .002 T.I.R.
8. COMPLETE THREAD TO EXTEND TO AT LEAST .085 OF HEAD.
9. ALL DIMENSIONS TO BE MET AFTER PLATING WITH .0002 - .0005 DULL NICKEL.
10. UNIT MUST NOT BE DAMAGED BY A 30 IN. LB. TORQUE APPLIED TO A FULLY ENGAGED 1/4-28 UNF-2B FULL NUT ASSEMBLED ON THREADS. AFTER APPLICATION OF TORQUE THREADS MUST FIT INTO A "GO" GAUGE.
11. THE USE OF AN EYELET WITH THE GLASS INSULATED PIN IS ACCEPTABLE PROVIDED THE MAX. O.D. DOES NOT EXCEED .085.
12. GLASS AND/OR EYELET NOT TO PROTRUDE ABOVE FACE "A".
13. UNITS TO BE BURR AND CHIP-FREE AND SO PACKAGED FOR SHIPMENT AS TO PREVENT BENT PINS OR DAMAGED THREADS.
14. ~~THIS DRAWING SIMILAR TO C10546.~~

C65010

FIG. 2.2.2 STUD BASE
25 W, 100 MC AMPLIFIER



LET.	REVISIONS				
A	350/345 WAS .352/.348	—			
B	B1, WAS .452; B2, ADD: TOL PER SIMILAR TO C14830				
	B3, ADDED (SHEET)				

11.- THE THREE INSULATED PINS SHALL HAVE AN ELECTRICAL RESISTANCE BETWEEN PIN & STUD OF 10 KILOHMS OHMS MIN.

10. NICKEL PLATING ON BODY TO WITHSTAND 300°C FOR 1000 HOURS WITHOUT VISIBLE DETERIORATION.

9. ALL DIMENSIONS MEASURED AFTER PLATING.

8. DEPTH 'D' SHALL BE .457 MIN. AS MEASURED WITH A .037 DIA PIN INSERTED INTO THE TUBE.

7. MELTING POINT OF BRAZE USED MUST BE MORE THAN 500 C.

6. STAMP AS SHOWN LETTERS: E, B & C .06" HIGH. GOTHIC STYLE.

5. LEAK TEST: TEMPERATURE CYCLE 5 TIMES -55°C, 25 C, 300°C, 25°C, AND SO ON, THEN CHECK FOR A LEAK RATE TO BE LESS THAN 5×10^{-8} CC/SEC AS MEASURED BY A HELIUM LEAK DETECTOR UNDER ONE ATMOSPHERE PRESSURE DIFFERENTIAL.

4. TWIST TEST: GLASS MUST WITHSTAND WITHOUT DETERIORATION TO THE SEAL A 20 INCH - OUNCE TORQUE APPLIED 1/4' FROM GLASS.

3. TUBES TO BE HERMETICALLY SEALED & FREE OF FOREIGN IMPURITIES INSIDE. IF BRAZING IS USED FOR SEALING, THERE SHALL BE NO FLUX USED INSIDE THE TUBES. BODY SHALL BE NICKEL PLATED PRIOR TO FIRING. AFTER FIRING THERE SHALL BE NO PLATING OR OTHER CHEMICAL TREATMENT OF PARTS BUT THEY SHALL BE SEALED IN PLASTIC BAGS TO PREVENT FOREIGN MATERIALS FROM ENTERING TUBES.

2. MATERIAL: BODY: C. R. S.
INSULATOR: GLASS
TUBE: NICKEL-IRON ALLOY

1. BREAK ALL EDGES AND CORNERS .010 RAD. MAX.

NOTES:

C65011

FIG. 2.2.3 CAP
25 W, 100 MC AMPLIFIER

path problems and frequency problems, discussed in Paragraph 2.4 of this chapter, is improved sufficiently, it should then become possible to make significant improvements in the device performance by altering either the device design or the actual processes used in making the device. At present, alterations in device design are considered to be far less beneficial than concentrating on work involved in processing and package improvements.

2.3 Process Development

While the N+ diffusion presently employed as a collector contact is quite satisfactory, the state-of-the-art of epitaxial materials is being continually reviewed for such usage. At such time as the epitaxial materials reach a stage of perfection which will yield leakage values comparable to those obtained with the diffused collector materials, the epitaxial materials will be incorporated into the 75 watt process. The use of the epitaxial material will enable somewhat better control over the collector thickness, and enable improved electrical and thermal performance, and increased yield during processing. Experience with planar diffusion techniques indicates that many of the device problems originate in or as a result of the oxide masking processes employed. Both the oxide thickness and impurity content have profound influence on the electrical characteristics of the device, particularly the leakage currents and the breakdown voltages. The problem is further complicated by the fact that the original oxide is subsequently modified by later diffusion processes and assembly operations. The original collector oxide is reconstituted and

p-type impurity is added during the base deposition and distribution. It would be naive to assume that the remaining processing would not also have effects. The base, emitter, and metallizing oxides should also be altered in a similiar manner. In addition to the thickness and impurity content, the coverage necessary to ensure masking from subsequent diffusions may be incomplete due to the original conditions or following processing. Any defect of this sort can rapidly degrade the planar breakdown voltage characteristic. Work during the first quarter has been directed toward producing clean oxides with suitable thickness and complete diffusant coverage. The development of subsequent processes has as a prime requisite the maintainance of the original oxide in as clean and complete a state as is practical. Some consideration is also being given to removing the oxides in toto and replacing them with a new "clean" oxide prior to cutting the metallizing pattern. Work in this area has shown promise. The work in the area of producing improved oxides and maintaining them will continue and the results will be reported in the succeeding reports.

Since this is a PEM contract, the improvement of yield is a prime consideration. In addition to the control problems discussed above, the control of the diffusions themselves is of paramount importance. The depth of the diffusions has a direct bearing on the frequency performance, the breakdowns obtainable

and the power capabilities of the device. Should the diffusions go too deep, the oscillator and amplifier performance will be impaired and the h_{fe} will be lowered, while dc characteristics such as h_{FE} will still be attainable. In addition to the depths of diffusion the variation of those depths must be controlled to produce the required base width range which yields the specified h_{FE} and frequency characteristics. Only through this improved control will the higher yields, necessary to economical production of this device, be attained. Work during this quarter has also been expended toward maintaining the necessary temperature control and improving the uniformity of the deposited impurity. The present temperature control is considered good and the temperature is continually monitored to ensure that it remains that way. The improved uniformity of deposition is being sought through refinements of existing techniques as well as investigation of new and more promising methods, involving variations in old diffusant sources as well as several new possible diffusant source chemicals.

Another area of investigation which is peculiar to the planar process, but not directly related to the diffusion processes described above is that of photoresist masking. The problem here is one of mechanics of alignment. There are two main areas of endeavor, obtaining suitable masks and suitable equipment to align the masks with the work. Design considerations require an accuracy on the order of 1/2000 of an inch. This accuracy

must be maintained over an area of slightly more than three square inches. The problem here centers around the tendency of the accuracy of the pattern to "fall off" towards the edge of the pattern. As improved patterns are developed they are being incorporated into the process. The second area is the incorporation of an improved alignment apparatus. The present equipment is adequate, but could be improved in ease and speed of operation consistent with accuracy. The new apparatus should be more production-worthy from the standpoint of rate. The improved masks and improved ease of alignment of the patterns should also increase the yield to the specified device. This area is undergoing intensive investigation at present.

The metallizing of the base and emitter contacts is presently being accomplished by means of a gold, nickel, and silver electroless plating process. This technique is satisfactory, but the aluminum evaporated front contact offers better performance over a wider range of temperature. By virtue of evaporation and the subsequent alloying, a metallurgical bond to the silicon is obtained which is stronger than any available chemiplated bond. In addition to the stronger bond produced, the aluminum contact offers the possibility of storage at higher temperatures than the chemiplated bond can attain. Early work has indicated the need to build up the aluminum thickness in order to carry the currents involved. This increased aluminum thickness has created a control problem in the alloying. Some good work has

been accomplished in applying the aluminum metallizing, but much still needs to be done. The use of aluminum metallizing would also create a problem with the presently used gold lead wire, namely "purple plague". Preliminary work with aluminum lead wire and ultrasonic bonding appears promising, but has not been evaluated with respect to high frequency performance to date. Further developments will be described in subsequent reports.

The present crystal mounting process yields adequate results. But, in the interest of attaining and maintaining the lowest possible thermal resistance with the best possible production rate, the process is constantly being monitored to refine and control the various aspects which govern the electrical and thermal output characteristics. Effort is also being devoted to the improvement of the production rate by possible redesign of the process.

The current leadbonding process is also adequate in terms of the present metallizing, with the exception that rate improvement is desirable. As mentioned above, the use of aluminum metallizing would necessitate a change in the leadbonding material and process. Early work along the ultrasonic leadbonding of aluminum lead wires appears promising, both in producing a more reliable bond and in giving a faster production rate.

2.4 Package Design

The package presently being used, while it is the best available, suffers from two problem areas. The first problem is the complete electrical isolation of the transistor from the case. The required isolation has been accomplished by the use of a beryllium oxide isolation tab. Beryllium oxide was chosen since it offers the best combination of dielectric and thermal properties. The major problem centers in the fact that this is a state-of-the-art material. PSI has had continued difficulty obtaining properly metallized beryllium oxide isolation tabs. If tabs are used on which the initial metallizing is not fired properly, the devices using those tabs will fail on power dissipation. Examination of the failures has revealed that the typical mode is a complete separation between the beryllium oxide and the first metallized layer. This separation prevents the transfer of any heat and the device burns out. PSI is working closely with the suppliers to advance the art of ceramic metallizing and thereby to remedy the situation. Other areas which can contribute to the thermal path problem to a lesser degree are the brazing of the tab to the stud and the mounting of the crystal to the tab. These areas seem to be under relatively good control since a properly metallized tab yields quite satisfactory results.

The second problem with respect to the package is its frequency performance. This package was originally intended for use at lower frequencies where the effect of lead inductance was at a

minimum. At 100 megacycles the input to the device is inductive by virtue of the lead inductance rather than capacitive as one would expect from semiconductor device theory. This impairs the frequency performance significantly. New package designs are being considered which should improve the frequency performance, device reliability, and ease of fabrication. Several package designs are being checked out at present on other PSI high performance devices with promising results. It appears that in the case of high power - high frequency devices it is an absolute necessity to spend as much time on the electrical and thermal characteristics of the package as on the characteristics of the silicon transistor. This area of endeavor is now our prime consideration as all possible efforts at producing a package worthy of the device are being made.

CHAPTER 3

Product Engineering

3.1 Introduction

Until such time as a final processing procedure is decided upon a detailed pilot line structure is extremely difficult to determine. However, as a preliminary step in establishing a pilot line facility, a generalized block diagram is being prepared.

During the course of the work on the 25W-100MC Research and Development Program, Contract No. DA 36-039 SC-87342, a processing procedure was evolved based on the present package and crystal design. While current design is capable of meeting the desired specifications on the 75W transistor it is difficult to obtain a high yield process. In order to fulfill both letter and spirit of this contract it is felt that a basic redesign of package and crystal coupled with processing changes to enable higher yields is a necessity.

For example, our current metallizing process is a chemical plating process. Evidence accumulated on a company funded metallizing program indicated a newly developed evaporative metallizing technique utilizing aluminum in connection with an ultrasonic bonding

method would have a higher yield and a greater throughput rate with reduced operator personnel. This evidence must now be verified on 25W-100MC devices, details of the process worked out, electrical characteristics determined and the necessary equipment selected, purchased and installed.

Test equipment is discussed in Paragraph 3.2 of this chapter. The various types of test equipment which we will need are already known. However, in order to determine placements and amounts of equipment, some information must be generated as to yield to various parameters during testing. This information will be generated by producing the engineering and preproduction samples called for by the contract. The problem boils down to one of fixing the processes and ordering such equipment as is not already on hand. In general the equipment is known but the necessary modifications have not yet been sufficiently fixed. The area of equipment best understood is the electrical test gear, and this is discussed in the following section.

3.2 Test Equipment

Currently on hand in the area of test equipment is an inventory of at least one piece for each type needed. Circuits have been built for both oscillator and amplifier performance and are presently undergoing intensive testing. However, to specify designs on jigs and fixtures one must first peg the package design and this remains to be done. In addition the actual number needed

of any particular test fixture must wait until a reasonable idea of our yield picture is developed.

The tests for V_{CBO} and V_{EBO} (or I_{CBO} and I_{EBO}) are performed on a Tektronix 575 curve tracer with suitably modified test sockets. These tests are not performed solely on completed units, but are utilized as in-process tests during diffusion and metallizing operations. As a result, several will be needed during the pilot run. These will be drawn from in-plant inventory as this equipment is general purpose in nature.

Tests for I_{CES} are also performable on a 575 curve tracer. To eliminate operator error and in the interests of speeding up the testing procedure special switch boxes have been designed and prototypes built to allow I_{CES}, V_{EBO}, and V_{CBO} and other low level pulse and D.C. tests to be carried out on a 575.

The test for static forward-current transfer ratio (h_{FE}) is carried out at two levels of power, 75 watts and 50 watts. This means that the units must have excellent heat sinks or that a pulsed h_{FE} tester with a short duty cycle be used. PSI has, in the transistor division, an h_{FE} tester with 2% duty cycle and a pulse width of 100μ/sec. There also exists - in the drawing board stage - a design for a heat sink suitable for continuous testing. The contractor intends to look at both techniques from a standpoint of speed, reliability and yield. At this moment it is quite

possible that both methods may be in use at the time of the pilot run.

The test for LV_{CES} is also easily performed using a Tektronix 575 with suitable high power adaptation. Such an instrument is available for use by the 75W-PEM pilot line.

Tests for collector-emitter saturation voltage are currently being performed for the 25W-100MC transistor Research and Development Contract. The equipment now in use on the above contract will be made available to the 75W-PEM contract.

Power gain at 100MC is the test of most interest to any potential user of this device. To that end the Research and Development Department at PSI developed for the 25W-100MC R and D contract an accurate 100MC neutralized common emitter amplifier circuit (see Figure 3.2.1) which has been in operation for several months and has proven to be most satisfactory. This circuit is so set up as to accept both capped and un-capped devices and as a result of this test it has been discovered that the package utilized by PSI is costing several db in potential power gain at 100MC. It is this discovery as well as the discovery of thermal path problem that has led to the package program discussed in Paragraph 2.4.

Second in interest only to power gain at 100MC is power oscillator performance. A circuit has recently been built at PSI for the purpose of testing oscillator performance at 100MC, although this test circuit configuration is not yet completely finalized. The present circuit is shown in Figure 3.2.2.

The measurement of base spreading resistance is being performed on the current 25W-100MC R and D contract. The equipment, built around a General Radio Transfer Function Bridge, is satisfactory but the technique used is slow. Efforts at producing a streamlined procedure are underway.

PSI at present is set up for testing output capacitance at a frequency of some 140 kc and therefore must modify its equipment to attain 1 mc collector capacitance measurements.

Small signal measurements of the short-circuit forward-current transfer ratio are already made on the 5W-70MC transistor being produced at PSI under Production Engineering Measure Contract No. DA 36-039 SC-85960 using the test schematic shown in Figure 3.2.0. Note that the tester was designed to make both 70 and 100MC measurements. This equipment will serve as the prototype for h_{fe} test positions on the pilot line.

In conclusion, a general determination of needed equipment types has been made. A prototype or working model of each kind of test piece is available and undergoing investigation. However, jigs and fixtures depending on package configuration cannot be fixed until the package is. In addition, order of "x" number of pieces of equipment must wait until yield analysis tells the equipment engineer what "x" number will be.

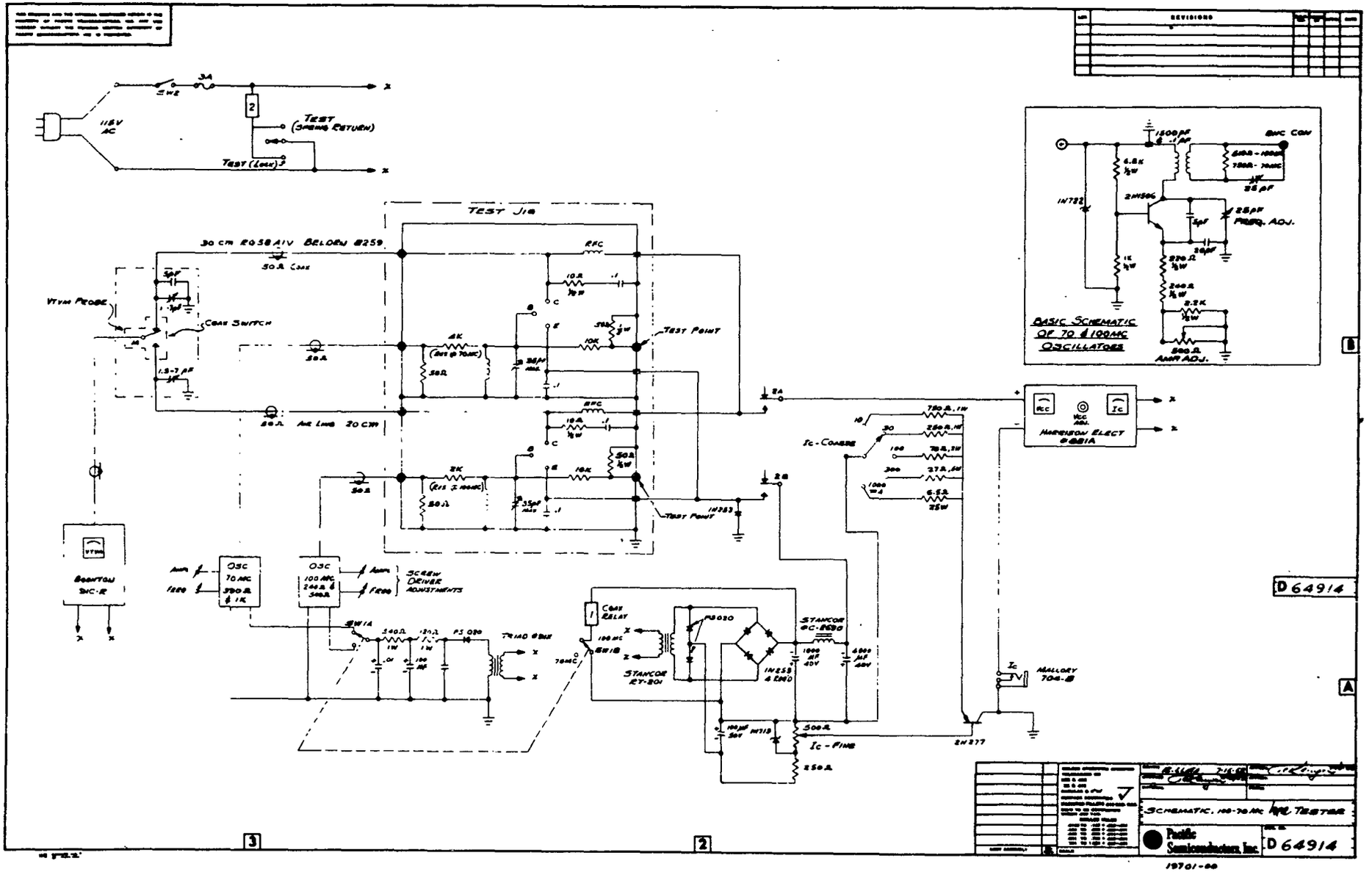
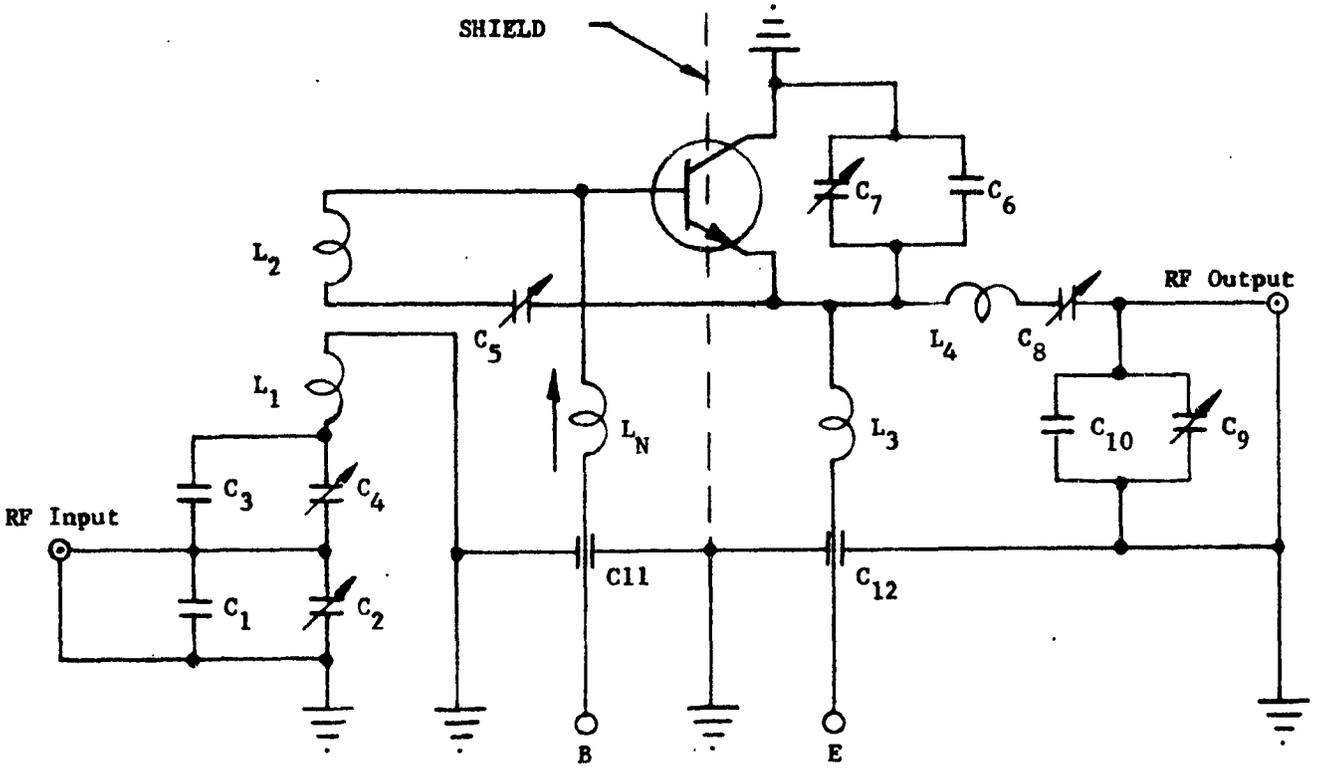

TEST JIG
BASIC SCHEMATIC OF 70 & 100MC OSCILLATORS
SCHEMATIC, 100-70 MC TYPE TESTER
Pacific Semiconductors, Inc.
D 64914

FIGURE 3.2.0



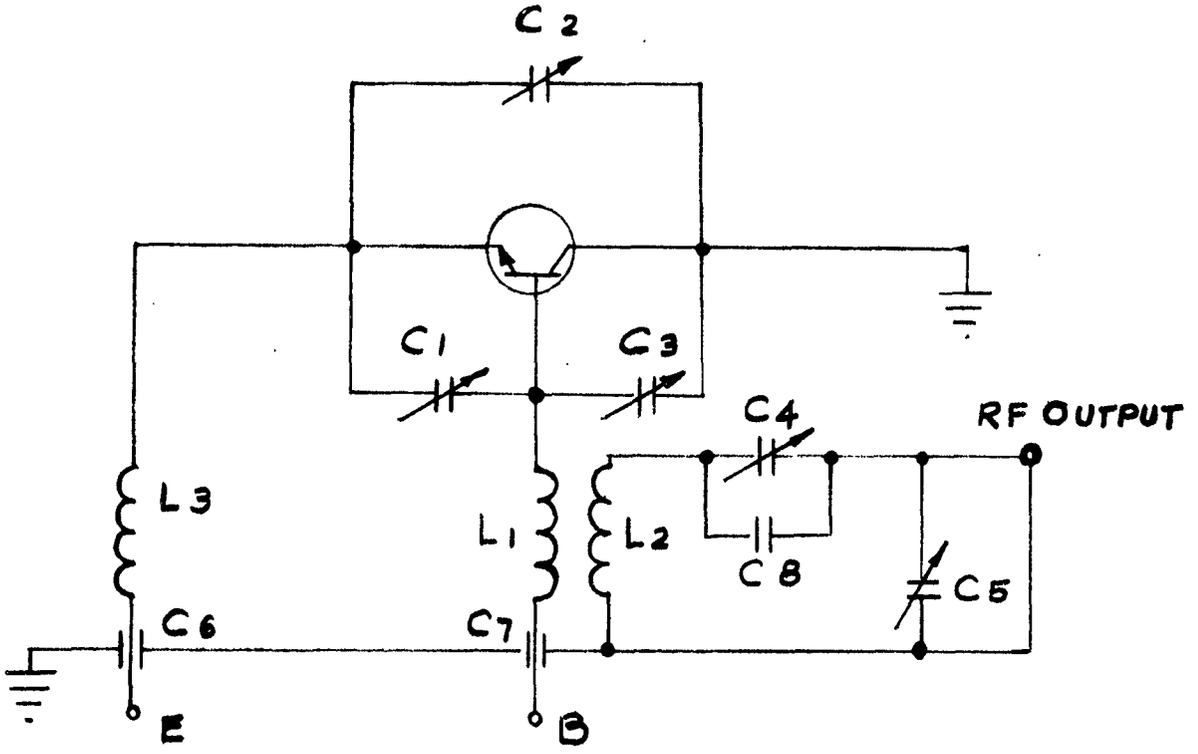
PARTS LIST

C_1	30 pf	Mica	Arco-Elmenco
C_2	3.7-52 pf	HF-50	Hammarlund
C_3, C_{10}	15 pf	Mica	Arco-Elmenco
C_4, C_5	3.2-50 pf	MAPC-50-B	Hammarlund
C_8, C_9	3.2-50 pf	MAPC-50-B	Hammarlund
C_6	10 pf	Mica	Arco-Elmenco
C_7	2.8-17.5 pf	HF-50	Hammarlund
C_{11}, C_{12}	2300 pf	Feedthru	Centralab

L_1	3 turns, No. 14 Insulated Copper Wire wound on 1/4" Plastic Rod.	L_3	2 turns, No. 14 Silver-coated Copper Wire wound 1/4" diameter and tapped quarter-turn from Emitter.
L_2	1-1/2 turns, No. 14 Silver-coated Copper Wire tightly coupled by interwinding with L_1 in phase.	L_4	2-1/2 turns No. 14 Silver-coated Copper Wire wound 1/4" diameter.
L_N	4 turns, No. 18 Silver-coated Copper Wire wound on 1/4" Mica Form Slug Tuned.		

100 MC NEUTRALIZED COMMON EMITTER
AMPLIFIER CIRCUIT

FIGURE 3.2.1



PARTS LIST

C_1	3.2 - 50 pf	Air Padding	E.F. Johnson Co.
C_2	2.5 - 7 pf	Mica	CRL CentraLab
C_3	1 - 12 pf	Ceramic	Arco-El Menco
C_4 and C_5	2.9 - 35 pf	MAPC-35-B	Hammerlund
C_6 and C_7	2300 pf	Feedthru	CentraLab
C_8	20 pf	Mica	El Menco

L_1 - 2-1/2 turns, No. 14 (AWG.) silver-coated copper wire wound on 1/4" ceramic form, slug tuned.

L_2 - 3-1/2 turns, No. 14 insulated copper wire tightly coupled by interwinding 1/2 turn with L_1.

L_3 - 1 μh RFC Coil Miller

100 MC OSCILLATOR

FIGURE 3.2.2

SECTION IV - SUMMARY AND CONCLUSION

The first interval of this contract has been spent in:

1) Making feasibility experiments concerned with production process changes in the light of improving throughput yield and device reliability.

2) Evaluating different package designs in an attempt to eliminate potential problems in frequency performance and a severe thermal path problem encountered in the 25W-100MC Research and Development Contract.

3) Investigating new processing equipment due to changes because of the above-mentioned steps.

4) Testing electrical circuits used in test check-out of the transistor.

PSI proposes to make changes in three areas which encompass device design in the broadest sense of the word. Improvements can be made in current processes, in the package design and in device design of the silicon crystal. By making these changes not only will a production-worthy device be created, but the additional - and highly useful - benefits will accrue of improved performance and reliability.

The changes in device design are perhaps the least important at this time. Some work on device design will be of an analytical

nature, such as the proposed h_{fe}, power gain and output study.

Once the relationships between h_{fe} and power output or gain are understood a directed advance on device limitations becomes possible. Changes made possible by use of epitaxial instead of triple diffused processes and by use of improved geometry would give a much improved device and fall into the area of the device designer.

A major increase in yield comes through processes improvement. Improved mask oxidation technique, metallizing operation and passivating processes would make for greater ease in production and greater predictability as devices.

By far the biggest and most beneficial change possible at the moment is the change in package. It cannot be said too often that package and silicon crystal must be designed for one another - not separately. At present the 25W-100MC crystal is far superior in design and performance to its package, which is plagued by poor thermal path due to BeO problems and by poor high frequency performance, due to inadequate mechanical-electrical design.

Initial blocking out of pilot line equipment needs has been completed. Final determination of the new process changes will be needed before it will be possible to provide detail pilot line

process and equipment layouts.

Determination of required test equipment has been made, and most of the required equipment is already on hand or available as prototypes. Schematics are included in this report for several pieces of high frequency gear called for in the design specifications (see Appendix). This equipment is already available and is currently operating quite satisfactorily while in use for the 25W-100MC Research and Development Contract.

SECTION V - PROGRAM FOR THE NEXT INTERVAL

The program for the next interval will encompass the following areas of endeavor:

1) Continue package evaluation and design study.

2) Continue investigations into refinement of present diffusion techniques and investigate new diffusion techniques where applicable.

3) Continue the work to obtain increased control over the photoresist operations wherever possible.

4) Continue the evaluation and refinement of aluminum metallizing and the assoicated aluminum leadbonding.

5) Continue the co-ordination with suppliers to improve the state-of-the-art beryllium oxide tab quality.

SECTION VI - PUBLICATIONS, REPORTS, AND CONFERENCES

There were no publications or conferences applicable to this contract during this quarter.

The first monthly letter report was submitted 10 August 1962.
The second monthly letter report was submitted 14 September 1962.
The third monthly letter report was submitted 11 October 1962.

SECTION VII - IDENTIFICATION OF PERSONNEL AND EXPENDITURES

The following professional personnel have been assigned to work on the 25W-100MC PEM contract.

Ronald N. Clarke

Mr. Clarke has four and one-half years experience in semiconductors (all with PSI) and spent three and one-half years as a Fleet technician with the U.S. Navy. He received an A.A. degree from San Mateo Junior College and a B.A. degree in Physics from the University of California.

Mr. Clarke joined PSI upon graduation and was engaged in process work for diodes. He later became the Diffused Diode Product Engineer, further improving the computer diode developed on a Signal Corps contract. At a leter date he was responsible for the development of an advanced high reliability computer diode for Minuteman.

Mr. Clarke was then transferred to the Diode Engineering Group where he had the responsibility for the Signal Corps Variable Capacitor Diode Contract. While in the Diode Engineering Group, he was also involved in advanced process development

Early this year, Mr. Clarke was transferred to the Research and Development Diode Group where he worked on an improved version of the diffused computer diode. Recently he has moved into the Development and Engineering Transistor Group where he now has the responsibility for the 5W-70MC technical co-ordination.

William D. Gray

Mr. Gray has ten years of technical experience, plus two years experience as a military instructor. He attended El Camino College, Army Engineering School, Fort Belvoir, Ve., U.C.L.A. and West Coast University, majoring in electrical engineering.

Mr. Gray was associated with Servomechanisms, Inc., Los Angeles, California, for seven years, where he was supervisor of the Ground Support Test Equipment Group, and was responsible for design of military test equipment.

Mr. Gray joined Pacific Semiconductors, Inc. in February 1960. He has since been concerned with the design of VHF transistor packages, thermal dissipation studies, and investigation of various types of glass-to-metal sealing techniques. In October of 1962, he was promoted to Section Head, Package Engineering.

He is a member of the American Ceramics Society.

Richard C. Neville

B.S.E.E. and M.S.E.E. - California Institute of Technology

Mr. Neville joined PSI in 1959 directly from Cal Tech where he graduated with honors, specializing in Semiconductor Physics and Electronics. He was initially assigned to our VHF Transistor Development Group where he became an expert in diffusion processes. Mr. Neville has also had device design assignments in both diode and transistor development programs of high-speed switching devices, including the 2N706, 2N708 and a 5-watt, 500MC VHF transistors. In July 1961 he joined the PNP Transistor Group, becoming its project leader in March 1962. In connection with this effort he directed studies concerned with device design (2N1132b) evaluation of epitaxial material, metallizing techniques, and oxide properties. He is also concerned with the PSI transistor Failure Analysis Program. In conjunction with this work he has performed studies on radiation damage to silicon devices.

Mr. Neville is a member of the IRE and Tau Beta Pi.

Michael O. Preletz

Mr. Preletz received his B.S. degree in Military Engineering from the United Stated Military Academy in 1960. After serving as a lieutenant in the army artillery he joined the Western Electric Company, where he worked on low and medium power NPN

mesa transistors. During this time he was doing graduate electrical engineering work at Lehigh University.

In May 1962 Mr. Preletz joined Pacific Semiconductors, Inc. He is presently concerned with diffusion and photoresist process engineering of VHF medium power transistors.

Bernard Rappaport

Mr. Rappaport has had eleven years of experience in the fabrication of electronic and electromechanical components and production engineering of semiconductor devices.

Mr. Rappaport received his B.A. degree in Physics in 1949 from the University of California at Los Angeles. He attended the graduate school at the University of Southern California, where he also taught electricity and magnetism. He engaged in microclimatology research in 1950 and 1951. He then became a project engineer and pilot line supervisor for the namufacture of miniaturized electromechanical devices.

Mr. Rappaport joined Pacific Semiconductors, Inc. in 1956 and assumed pilot line responsibility for the Industrial Preparedness Study of Diffused Silicon High Speed Computer Diodes (Contract No. 36-039 SC-70274). He was active in the program to extend the diffusion diode family and in the high voltage silicon cartridge rectifier program. He later directed the pilot manufacturing facility, mechanical and electronic equipment procurement and

package engineering programs for all new products within the Transistor Division.

Mr. Rappaport is presently Head of the Transistor Final Development Group in the Research and Development Department.

David H. Treleaven

Mr. Treleaven received his B.A. Sc. in Engineering Physics from the University of British Columbia in 1962. He joined Pacific Semiconductors Inc. in September 1962 and since has been working on the 5W-70MC and 25W-100MC device fabrication.

Mr. Treleaven is affiliated with Delta Upsilon.

Man-Hour Labor Expenditures

Effort expended by professional employees:

Name	Hours
L. L. Ornik	56
G. Otto	412
J. Podell	36
M. O. Preletz	152
D. H. Treleaven	80
W. M. Wilson	96
TOTAL	832
Effort expended by technicians	1202
TOTAL	2034

APPENDIX

TRANSISTOR, SILICON, VHF, POWER (75 WATT) TYPE SigC-2N(X-6)

1. SCOPE

1.1 Scope. - This document covers the detail requirements for silicon, VHF, Power Transistors capable of delivering 25 watts of output power with 10 db of power gain at 100 mc.

1.2 Maximum ratings at 25°C. (See 3.2 herein):

BV_{CBO}	BV_{CES}	BV_{EBO}	I_C	P_C	T_j	T_{stg}
Vdc	Vdc	Vdc	Adc	W	°C	°C
180	180	5	1.5	75 (at: T_C= 25°C)	200	-65 to + 200

2. APPLICABLE DOCUMENTS

2.1 The following documents, of the issue in effect on date of invitation for bias, form a part of this specification to the extent specified herein:

SPECIFICATIONS

MILITARY

MIL-F-14072	Finishes For Ground Signal Equipment
MIL-S-19500	Semiconductor Devices, General Specification For

STANDARDS

MILITARY

MIL-STD-202	Test Methods For Electronic and Electrical Component Parts

DRAWINGS

SIGNAL CORPS

SC-A-46600 Preproduction Sample Approval in Lieu of Requirements in Specifications.

(Copies of specifications, standards, drawings, and publications required by contractors in connection with specific procurement functions should be obtained from the procuring agency or as directed by the contracting officer. Both the title and number or symbol should be stipulated when requesting copies.)

3. REQUIREMENTS

3.1 Requirements.- Requirements for the transistors shall be in accordance with Specification MIL-S-19500 and as specified herein.

3.2 Abbreviations and symbols.- The abbreviations and symbols used herein are defined in Specification MIL-S-19500 and as follows:

P_i . . . . . power input

P_o . . . . . .power output

LV_{CES} . . . . . sustaining voltage (collector-to-emitter) base short-circuited

3.3 Design and construction.- The design and construction of the transistors shall be in accordance with applicable requirements of Specification MIL-S-19500.

3.3.1 Transistor case.- The transistor case shall incorporate a stud with a mounting nut and lock washer, physically located at the end of the case opposite the leads, to enable ready mounting of the transistor and dissipating the required power. The transistor case shall be electrically insulated from the collector, emitter, and base.

3.3.2 Operating position. - The transistors shall be capable of proper operation in any position.

3.3.3 Finishing of external metallic surfaces.- The finishing of external metallic surfaces shall be in accordance with requirements in Specification MIL-F-14072 for surface classification Type II, except that the requirements in Specification MIL-F-14072, Section 3, Requirements, covering moisture resistance and finish resistance, and Section 4, Quality Assurance Provisions therein, shall not be applicable. If, due to

special conditions of service or design, a contractor desires to use finishes, materials, or processes other than those specified, such proposal including the reasons therefore shall be submitted to the Contracting Officer for approval. At the discretion of the Contracting Officer, samples and test data may be required to substantiate the suitability of the proposed substitute(s).

3.4 Performance characteristics.- The transistor performance characteristics shall be as specified in Tables I and 11 herein. (See 6.3 herein.)

3.5 Marking.- The transistors shall be marked in accordance with Specification MIL-S-19500 and as follows. In instances where the diminutive size or lack of suitable surface area on the device would prevent a marking accomplishment readable by the unaided eye, 20/20 vision, at eight inches distance from the device, such marking may be omitted directly on the device. All required marking shall be placed on the unit package.

3.5.1 Type-designation marking.- The transistors shall be marked with the letters "SigC" and the "2N" designation of the device. The "2N" designation of the device shall be "(X-6)" until an identification number conforming to the type designation requirements of Specification MIL-S-19500 has been established.

4. QUALITY ASSURANCE PROVISIONS

4.1 General. - Except as otherwise specified herein, the responsibility for inspection, general procedures for acceptance, classification of inspection, and inspection conditions and methods of test shall be in accordance with Specification MIL-S-19500, Quality Assurance Provisions.

4.2 Preproduction Sample Approval. - The Preproduction Sample approval requirements in Signal Corps Drawing SC-A-46600 hereby replace any Qualification requirements referable to the product covered herein.

4.3 Sampling and acceptance criteria for Acceptance Inspection (see 6.2 herein).- For all tests except Life tests, sampling and acceptance criteria shall be in accordance with 4.3.1 and 4.3.2, respectively, herein for Life tests, sampling and acceptance criteria shall be in accordance with requirements for Method B in Specification MIL-S-19500, Appendix C. The respective LTPD (Lot Tolerance Percent Defective) and Max. Acc. No. (Maximum Acceptance Number) requirements in Tables I and 11 herein shall govern relative to the details in 4.3.1 and 4.3.2 herein.

4.3.1 Sample Size. - The sample size shall be selected by the manufacturer using Table III herein. The sample size so chosen shall be within the Max. Acc. No. limit associated with the LTPD specified in Tables I and II herein.

4.3.2 Sample acceptance criteria.- For the sample size tested, the Acceptance Number "(a)" in Table III shall not be exceeded. (Rejection number "r" = "(a)" + 1.)

4.4.4 Tightened inspection.- Tightened inspection on resubmitted lots is obtained by testing to an LTPD equal to or less than one-half of the specified initial LTPD.

4.4 Specified LTPD and Max. Acc. No.- The LTPD and Max. Acc. No. specified for a subgroup in Tables I and II herein shall apply for all of the tests, combined, in the subgroup.

4.5 Destructive tests.- The Group B, Subgroups 2, 3, 4, 5, 6, and 7 tests are considered destructive. However, the tests of Subgroups 2, 3, 4, 5, 6, and 7 can be considered non-destructive if sufficient evidence is presented to the Government inspection authority to that effect. Acceptable evidence, for example, would be repeating of all Subgroups 2, 3, 4, 5, 6, and 7 tests, ten times, without significant device degradation. This test repetition procedure need be done only once at inception of Acceptance Inspection, provided that no change in design, or of production techniques, has been effected.

4.6 Disposition of sample units.- Sample units that have been subjected to and have passed Group B, Subgroups 2, 3, 4, 5, 6 and 7 tests not determined to be destructive tests may be delivered on the contract sample units are subjected to and pass Group A inspection. Defective units from any sample group that may have passed group inspection shall not be delivered on the contract or order until the defect(s) has been remedied to the satisfaction of the Government.

4.7 Particular examination and test procedures.-

4.7.1 Sustaining Voltage Test. - The sustaining voltage of the collector with respect to the emitter shall be measured under the conditions specified, with the base short-circuited to the emitter.

4.7.2 Oscillator Power Output Test.- The specified voltage and current shall be applied to the respective terminals under the conditions specified and the power output of the oscillator shall be measured at the frequency specified.

4.7.3 Base Spreading Resistance test.- The specified voltage and current shall be applied to the respective terminals, with the transistor in the common-emitter configuration. An a-c small signal of the high frequency specified shall be applied to the input terminals, and the output terminals shall be short-circuited. The real part of the short-circuit input impedance shall be measured and assumed equal to the base spreading resistance.

4.7.4 Tension test.- The specified force shall be applied to each

lead in the direction of the axis of the lead. The force shall not be applied to more than one lead at a time, and all leads shall be tested.

4.7.5 Torque Test.- The specified torque shall be applied to the stud and about its axis. The stud shall not have become loosened nor the threads damaged, as a result of this test.

4.7.6 Bending Moment test - The transistor shall be mounted by the normal mounting means. The specified force shall be applied, without shock, at right angles to the lead and near the end of the lead.

Table 1. Group A Inspection

MIL-S-19500 Approx. C Ref. Par.	Examination or Test	Conditions	LTPD	Max. Acc. No.	Symbol	Limits Min.	Limits Max.	Unit
	Subgroup I		Major:5 Minor:10	3 4				
30.13	Visual and mechanical Examination	---			---	---	---	---
	Subgroup II		5	3				
50.6	Collector cutoff current	V_{CB} = 180Vdc I_E = 0			I_{CBO}	---	5	mAdc
50.6	Emitter cutoff current	V_{EB} = 5 Vdc I_C = 0			I_{EBO}	---	5	mAdc
50.9	Collector cutoff current	V_{CE} = 180Vdc V_{EB} = 0			I_{CES}	---	5	mAdc
50.9	Collector cutoff current	V_{CE} = 70Vdc V_{EB} = 0			I_{CES}	---	1	mAdc
50.40	Static forward-current Transfer ratio	V_{CE} = 50Vdc I_C = 1.5Adc			h_{FE}	10	---	---
50.40	Static forward-current Transfer ratio	V_{CE} = 70Vdc I_C = 715mAdc			h_{FE}	15	45	---
1/	Sustaining Voltage	I_C = 100mAdc V_{EB} = 0			LV_{CES}	90	---	Vdc
50.25	Saturation Voltage	I_C = 1.5Adc I_B = 300mAdc			$V_{CE(SAT)}$	---	0.75	Vdc

Table 1. Group A Inspection - (Continued)

MIL-S-19500 Appx. C. Ref. Par.	Examination or Test	Conditions	LTPD	Max. Acc. No.	Symbol	Limits Min.	Limits Max.	Unit
	Subgroup 3		5	3				
50.15	Power Gain	V_{CE} = 70Vdc I_C = 715mAdc f = 100mc P_i = 2.5W $T_c \leq 55^{\circ}C$ 2/			P_g	10	---	db
3/	Oscillator power output	V_{CE} = 70Vdc I_C = 715mAdc f = 100mc $T_C \leq 55^{\circ}C$			P_o	25	---	W
4/	Base Spreading Resistance	V_{CE} = 70Vdc I_C = 715mAdc f = 100mc			r'_b	---	10	ohms
50.19	Output Capacitance	V_{CB} = 70Vdc I_E = 0 f = 1mc			C_{ob}	---	25	μμf
50.33	Small-signal short-circuit forward-current transfer ratio	V_{CE} = 70Vdc I_C = 715mAdc f = 100mc			h_{fe}	7	---	db

1/ See 4.7.1 herein.
2/ Test Circuit as mutually acceptable to Contracting Officer's Technical Representative and contractor.
3/ See 4.7.2 herein. Test circuit as mutually acceptable to Contracting Officer's Technical Representative and contractor.
4/ See 4.7.3 herein.

Table II. Group B Inspection

MIL-S-19500 Appx. C Ref. Par.	Examination or Test	Conditions	LTPD	Max. Acc. No.	Symbol	Limits Min.	Limits Max.	Unit
	Subgroup I		10	2				
30.9	Physical dimensions	---						
	Subgroup II		10	3				
40.12	Solderability	---			---	---	---	---
40.14	Temperature Cycling	$T_{(high)}$ = +200°C Test Cond. C 1/			---	---	---	---
40.16	Thermal Shock	$T_{(high)}$ = 100° ± 3°C $T_{(low)}$ = 0° ± 2°C			---	---	---	---
40.6	Moisture Resistance	No initial conditioning			---	---	---	---
	End-point tests:							
50.9	Collector cutoff current	V_{CE} = 180Vdc V_{EB} = 0			I_{CES}	---	10	mAdc
50.9	Collector cutoff current	V_{CE} = 70Vdc V_{EB} = 0			I_{CES}	---	2	mAdc
50.6	Emitter cutoff current	V_{EB} = 5Vdc I_C = 0			I_{EBO}	---	10	mAdc
50.40	Static forward-current Transfer Ratio	V_{CE} = 70Vdc I_C = 715mAdc			h_{FE}	13	50	---

Table II Group B Inspection - (Continued)

MIL-S-19500 Appx. C. Ref. Par.	Examination or Test	Conditions	LTPD	Max. Acc. No.	Symbol	Limits Min.	Limits Max.	Unit
	Subgroup 3		10	3				
40.10	Shock	Non-operating 5 blows each in each orientation X1, Y1, Y2, Z1 (Total= 20 blows)			---	---	---	---
40.4	Constant acceleration (Centrifuge)	G = 20,000			---	---	---	---
40.18	Vibration, fatigue	V_{CB} = 20Vdc V_{EB} = 5Vdc			---	---	---	---
40.20	Vibration, variable frequency	---			---	---	---	---
	End-point Tests: Same as for Subgroup 2, above							
	Subgroup 4		10	3				
40.1	Barometric pressure (reduced)	Test Cond. B V_C-to-case = 180Vdc V_E-to-case = 180Vdc V_B-to-case = 180Vdc			---	---	---	---
30.6	High-temperature operation	T_A = + 150°C						
50.6	Collector cutoff current	V_{CB} = 70Vdc I_E = 0			I_{CBO}	---	10	mAdc

Table II. Group B Inspection - (continued)

MIL-S-19500 Appx. C. Ref. Par.	Examination or Test	Conditions	LTPD	Max. Acc. No.	Symbol	Limits Min.	Limits Max.	Unit
	Subgroup 4 - Cont'd)							
30.7	Low-temperature operation:	T_A = -55°C						
50.40	Static Forward-Current Transfer Ratio	V_{CE} = 70Vdc I_C = 715mAdc			h_{FE}	8	---	---
30.11	Thermal resistance	---			θ_{J-C}	---	2.33	°C/W
40.9	Salt spray (corrosion)	Test Cond. A			---	---	---	---
	End-point tests: Same as for Subgroup 2, Above							
	Subgroup 5		10	3				
40.15	Tension	Force = 5 lb. 2/			----	----	---	---
40.17	Torque	Torque = 30 in/lb. 3/			---	---	---	---
4/	Bending moment	Force = 1 lb.			---	---	---	---
	Subgroup 6		λ 5	3	---	---	---	---
40.7	Storage Life	Method B $T_{Stg.}$ ≙ +200°C			---	---	---	---
	End-point tests: Same as for Subgroup 2, above							

Table II. Group B Inspection - (Continued)

MIL-S-19500 Appx. C. Ref. Par.	Examination or Test	Conditions	LTPD	Max. Acc. No.	Symbol	Limits Min.	Limits Max.	Units
	Subgroup 7		$\lambda = 5$	3				
40.7	Operation Life	Method B V_{CB} = 20Vdc I_C = 350mA			---	---	---	---
	End-point Tests							
	Same as for Subgroup 2, Above							

1/ + Per Method 102A in Standard MIL-STD-202.

2/ See 4.7.4 herein

3/ See 4.7.5 herein

4/ See 4.7.6 herein.

5. PREPARATION FOR DELIVERY

5.1 Preparation for delivery. - Preparation for delivery shall be in accordance with Specification MIL-S-19500.

6. NOTES

6.1 Notes. - The notes included in Specification MIL-S-19500, except for those covering qualification (see 4.2 herein) and the following, are applicable to this document.

6.2 Ordering data. - If this document is used with the "C" or later issue of Specification MIL-S-19500 containing LTPD-method Acceptance Inspection requirements, the solicitation should indicate that the Acceptance Inspection LTPD-methods requirements in paragraphs 4.3 through 4.3.3 herein shall be considered superseded by the pertinent requirements in the "C" or later issue of Specification MIL-S-19500.

6.3 Establishment of Additional Tests and Parameters.- The resolution of any additional tests and parameters that will serve for optimum performance evaluation of the device relative to the application need is encouraged. It is expected that such determination(s) will be by mutual agreement between the contractor and the responsible Government agency, and will be included in the final acceptance criteria for the device. Pertinent electrical, physical, mechanical, and environmental test coverage in Specification MIL-S-19500 should be considered as a primary guide in this regard.

NOTICE: When Government drawings, specifications or other data are used for any purpose other than in connection with a definitely related Government procurement operation, the United States Government thereby incurs no responsibliity nor any obligation whatsoever; and the fact that the Government may have formulated, furnished, or in any way supplied the said drawings, specifications, or other data isnnot to be regarded by implication or otherwise as in any manner licensing the holder or any other person or corporation, or conveying any right or permission to manufacture, use, or sell any patented invention that may in any way be related thereto.

Table III. Minimum Size of Sample to be Tested to Assure, With 90% Confidence, an LTPD no Greater Than the LTPD Specified

Acceptance Number (a)	Maximum Percent Defective (LTPD) 1/								
	20	15	10	5	2	1	0.5	0.2	0.1
	Minimum Sample Sizes								
0	11 (0.46)	15 (0.34)	22 (0.23)	45 (0.11)	116 (0.04)	231 (0.02)	461 (0.01)	1152 (0.005)	2303 (0.002)
1	18 (2.0)	25 (1.4)	38 (0.94)	77 (0.46)	195 (0.18)	390 (0.09)	778 (0.045)	1946 (0.018)	3891 (0.009)
2	25 (3.4)	34 (2.24)	52 (1.6)	105 (0.78)	266 (0.31)	533 (0.15)	1065 (0.080)	2662 (0.031)	5323 (0.015)
3	32 (4.4)	43 (3.2)	65 (2.1)	132 (1.0)	333 (0.41)	668 (0.20)	1337 (0.10)	3341 (0.041)	6681 (0.018)
4	38 (5.3)	52 (3.9)	78 (2.6)	158 (1.3)	398 (0.50)	798 (0.25)	1599 (0.12)	3997 (0.049)	7994 (0.025)
5	45 (6,0)	60 (4.4)	91 (2.9)	184 (1.4)	462 (0.57)	927 (0.28)	1855 (0.14)	4638 (0.056)	9275 (0.028)
6	51 (6.6)	68 (4.9)	104 (3.2)	209 (1.6)	528 (0.62)	1054 (0.31)	2107 (0.155)	5267 (0.062)	10,533 (0.031)
7	57 (7.2)	77 (5.3)	116 (3.5)	234 (1.7)	589 (0.67)	1178 (0.34)	2355 (0.17)	5886 (0.067)	11,771 (0.034)
8	63 (7.7)	85 (5.6)	128 (3.7)	258 (1.8)	648 (0.72)	1300 (0.36)	2599 (0.18)	6498 (0.072	12,995 (0.036)
9	69 (8.1)	93 (8.0)	140 (3.9)	282 (1.9)	709 (0.77)	1421 (.038)	2842 (0.19)	7103 (0.077)	14,206 (0.038)
10	75 (8.4)	100 (6.3)	152 (411)	306 (2.0)	770 (0.80)	1541 (0.40)	3082 (0.20)	7704 (0.08)	15,407 (0.04)
(r = a + 1)	1/ The minimum quality (approximate AQL percent defective) required to accept (on the average) 19 to 20 lots is indicated in parentheses, respectively below, for information purposes only.								